REMARKS

Claims 15-18 stand rejected under 35 USC §101. Claims 1-2, 11 and 15 stand rejected under 35 USC §103(a) as being unpatentable over Swoboda et al., U.S. patent 6,643,803 in view of Torrey et al., U.S. patent 6,145,123. Claims 3-6, 8-10, 12-13 and 16-17 stand rejected under 35 USC §103(a) as being unpatentable over Swoboda et al., U.S. patent 6,643,803 and Torrey et al., U.S. patent 6,145,123 in view of Hoyle et al., U.S. patent 6,453,405. Claims 7, 14, and 18 stand rejected under 35 USC §103(a) as being unpatentable over Swoboda et al., U.S. patent 6,643,803, Torrey et al. 6,145,123, and Hoyle et al., U.S. patent 6,453,405 in view of DeAngelis et al., U.S. patent 5,226,153.

Claims 1-18 have been amended to more clearly state the invention. Reconsideration of claims 15-18, as amended, and withdrawal of the rejection of claims 15-18 under 35 USC §101 is respectfully requested.

Reconsideration and allowance of claims 1-18, as amended, is respectfully requested.

Swoboda et al., U.S. patent 6,643,803 discloses emulation and debug circuitry that can be incorporated into a variety of digital systems. A stop mode of operation is provided in which an associated processor stops processing instructions in response to a debug event. A real-time mode of operation is provided in which the processor stops processing background instructions in response to a debug event, but in which high priority interrupts are still processed. While running or suspended, the emulation circuitry can jam an instruction into the instruction register of the processor to

cause processor resources to be read or written on behalf of the emulation circuitry. An embodiment of a processor core is provided that is a programmable digital signal processor (DSP) with variable instruction length, offering both high code density and easy programming. Architecture and instruction set are optimized for low power consumption and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks. Column 4, lines 59-62 states: Debug Host 13 is a computer, typically a PC, running the user-interface for a target processor debugger. The debug host allows the user to issue high level commands such as "set breakpoint at function main( )" or "examine the contents of memory from 0x0 to 0x100". Column 26, lines 46-48 states: Preemptive mode. In preemptive mode, the DT-DMA mechanism forces the creation of a hole and performs the access. Column 28, lines 40-43 states: Interrupts must be enabled by both masks to interrupt the CPU when it is suspended, however, the global interrupt enable (INTM) is ignored. Suspending execution will add only one cycle to interrupt latency. As shown in FIG. 1, a JTAG interface 11 couples a target device 10 to a debug host 13.

Torrey et al., U.S. patent 6,145,123 discloses an information processing system such as a microprocessor that includes a processor core, a debug register circuit and a trace unit. The processor core is for processing information according to a program. The program includes a plurality of instructions for execution by the processor core. Each of the plurality of instructions has a corresponding address. The debug register circuit is coupled to the processor core. The debug register circuit includes a dedicated initiate trace breakpoint register coupled to receive and store an

initiate trace address and a dedicated terminate trace breakpoint register coupled to receive and store a terminate trace address. The trace unit is coupled to the debug register circuit and the processor core. The trace unit initiates a program trace responsive to the program accessing the initiate trace address. The trace unit terminates the program trace responsive to the program accessing the terminate trace address. The program trace includes information regarding the execution of the program by the microprocessor. Column 5, lines 25-27, and 45-60 states: As is described hereinafter, trace unit 140 is turned on/off by using breakpoint registers 154 of debug unit 150. ....Referring to FIG. 2, trace unit 140 includes trace controller 142, trace buffer 144, CPU interface 210, debug interface 220 and pad interface 230. Trace CPU interface 210 provides an interface to processor core 112. Trace debug interface 220 provides an interface to debug unit 150 (e.g., an IEEE-1149.1-1990 compliant JTAG debug circuit). Trace pad interface 230 provides a parallel interface to bus 147 to provide trace information from trace unit 140 to host system 170. Trace pad interface 230 and debug port 152 provide alternative trace outputs. Trace controller 142 includes control logic for storage and/or retrieval of trace information provided by processor 110 via CPU interface 210. Trace buffer 144 provides storage for the trace information. Trace buffer 144 is a dual-ported random access memory (RAM) design and is organized as 256 entries by 20 bits. Alternatively, trace buffer 144 may have 128 entries or any other number of entries.

Hoyle et al., U.S. patent 6,453,405 discloses adata processing system having a central processing unit (CPU) with address generation circuitry for accessing a

circular buffer region in a non-aligned manner is provided. The CPU has an instruction set architecture that is optimized for intensive numeric algorithm processing. The CPU has dual load/store units connected to dual memory ports of a memory controller. The CPU can execute two aligned data transfers each having a length of one byte, two bytes, four bytes, or eight bytes in parallel by executing two load/store instructions. The CPU can also execute a single non-aligned data transfer having a length of four bytes or eight bytes by executing a non-aligned load/store instruction that utilizes both memory ports. A data transfer address for each load/store instruction is formed by fetching the instruction (600), decoding the instruction (610) to determine instruction type, transfer data size, addressing mode and scaling selection. For a non-aligned instruction, after selectively scaling (620) an offset provided by the instruction and combining the selectively scaled offset with a base address value the resultant address is then augmented (640) by a line size associated with the instruction. For circular addressing mode, both the resultant address and the augmented address are bounded (650, 651) to stay within the circular buffer region and two aligned data items are accessed in parallel (652, 653) and a non-aligned data item is extracted (654) from the two aligned data items, such that the non-aligned data item wraps around the boundary of the circular buffer region. Column 3, lines 11-14 states: In another embodiment of the present invention, the address generation circuitry in the .D units is operable to form an address for non-aligned double word instructions by combining a base address value and an offset value.

DeAngelis et al., U.S. patent 5,226,153 discloses a monitor for selectively

detecting and recording conditions at selected points within a system during operation that includes trigger logic connected from first selected points and responsive to selected conditions occurring at each of the first points for generating corresponding trigger outputs representing the occurrence of the selected conditions and a silo bank memory having a sub-silo for each second point. Each sub-silo has a first sub-silo segment with data inputs connected from the corresponding second point for recording data from the second point and a second sub-silo segment with data inputs connected from a time stamp generator. Silo write control logic is responsive to the trigger outputs to write the data representing the conditions present at each second point and the time stamp output of the time stamp generator into the corresponding sub-silo segments of the silo bank upon occurrence of a corresponding trigger output so that each condition recorded in the silo bank memory as the result of a trigger output has associated with it the time stamp count representing the relative time of occurrence of the trigger output. Column 13, lines 10-28 states: As was previously mentioned, Trigger Control 38 includes a Time Stamp Generator (TSG) 100 which is essentially a counter which is initiated upon and by the occurrence of a TRIGS from TRIGDET 96 and TRIGREG 98. The count output of TSG 100 is written into SSL 50 at the start of each sampling operation after the occurrence of a trigger, at the same address location as the data from SYSBUS 18 being recorded in SSL 50, and is provided so that a user of Bus Monitor 12 may determine the relative times of occurrence of each trigger condition. The count from TSG 100 is also written into PSL 52 and XSL 54, depending upon which of the portions of Silo Bank 40 are recording data in a given sampling operation

of Bus Monitor 12, to aid in correlating the data stored in SSL 50, PSL 52 and XSL 54. The time stamp counts are again written into PSL 52 and XSL 54 at the same addresses as the data being concurrently recorded thereon.

Applicant's respectfully submit that each of the independent claims 1, 11, and 15, as amended is patentable over the references of record, including Swobada, Torrey, Hoyle, and DeAngelis.

Reconsideration and allowance of each of the pending claims 1-18, as amended, is respectfully requested. As amended, each of the independent claims 1, 11 and 15 is believed to more clearly define the invention and to be patentable over the records of record including Swobada, Torrey, Hoyle, and DeAngelis.

35 U.S.C. §103 requires that the invention as claimed be considered "as a whole" when considering whether the invention would have been obvious when it was made. Graham v. John Deere, 383 U.S. 1, 148 USPQ 459, 472 (1966). It is applicants' claimed invention which must be considered as a whole pursuant to 35 U.S.C. §103, and failure to consider the claimed invention as a whole is an error of law. In order for there to be a prima facie showing of obviousness under 35 U.S.C. §103, it is necessary that the references being combined in an attempt to demonstrate prima facie obviousness must themselves suggest the proposed combination. For a combination of prior art references to render an invention obvious, "[t]here must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination." In re Oetiker, 977 F.2d 1443, 1447, 24 USPQ2D 1443, 1446 (Fed. Cir. 1992). That one must point to some reason,

suggestion, or motivation to make a combination is not to say that the teaching must be explicit, but in order to render an invention obvious by the combination of prior art references, the prior art must contain some reason, suggestion, or motivation. It is impermissible to use the inventor's disclosure as a "road map" for selecting and combining prior art disclosures. In Interconnect Planning Corp. v. Feil 774 F.2d 1132, 1143, 227 USPQ 542, 551 (Fed. Cir. 1985), the Federal Circuit noted, "The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time."

Independent claim 1 recites a method for implementing atomic data tracing in a processor system including an auxiliary processor unit coupled to a central processor unit (CPU), using the auxiliary processor unit (APU) to perform the steps of: identifying a trace instruction. Independent claim 11 recites an apparatus for implementing atomic data tracing in a processor system including an auxiliary processor unit (APU) coupled to a central processor unit (CPU). Independent claim 15 recites a computer program product for implementing atomic data tracing in a processor system including an auxiliary processor unit (APU) coupled to a central processor unit (CPU).

To implement atomic data tracing often it is necessary to write information into one trace buffer from multiple threads of execution or from interrupt level in addition to thread level and to maintain coherency in the trace buffer the determination of the current trace entry and increment to the next trace entry must appear to be atomic. The present invention avoids the requirement of a different trace buffer for each of the threads and interrupt levels a function needs to trace from, and avoids required extra

overhead to perform the lock checks and retries of the lock of other known tracing arrangements.

Each of the independent claims 1, 11, and 15, as amended, more clearly define a trace instruction and a trace engine of the invention, and the steps performed by the auxiliary processor unit (APU) of the invention. Advantages are that the APU trace instruction can be executed at user level without having to switch into kernel context, as is usually the case with masking interrupts or suspending thread dispatching. Second, the data can be written into one trace buffer from multiple execution contexts. This eliminates having to merge multiple trace buffers in post processing steps. The process of tracing is also simplified since code does not need to determine which trace buffer to write into based on the context it is running in. By holding the data in the GPRs, the data is saved automatically as part of the operating system's normal context switch process.

Each of the independent claims 1, 11, and 15, as amended, define the said trace instruction including a primary op code and indicating General Purpose Registers (GPRs) containing information to identify a first GPR containing data to be written into a current trace entry of a trace buffer and to identify a set of trace engine registers defining a trace engine to use for said trace instruction; said trace engine including said trace buffer; said data to be written being saved automatically in at least one GPR including said first GPR during normal context switch processing.

These limitations as recited in independent claims 1, 11, and 15, as amended, are not disclosed or suggested by the combined teachings of Swobada,

Torrey, Hoyle, and DeAngelis.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. See MPEP §2143.

Applicants respectfully submit that the rejections of claims 1-2, 11, and 15 under 35 USC §103(a) fail to meet this first criteria. Applicant respectfully submits that there is no suggestion or motivation in the Swobada, Torrey, Hoyle, and DeAngelis references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. None of the Swobada, Torrey, Hoyle, and DeAngelis references disclose or remotely suggest the trace instruction, nor the trace engine as taught and recited in each of the independent claims 1, 11, and 15, as amended.

Thus, each of the independent claims 1, 11, and 15, as amended, is patentable.

As taught and claimed in the present invention, the APU identifies a trace instruction, the APU identifies information from the processors General Purpose Register (GPRs), indicated in the trace instruction, to determine what data to write into

a trace buffer, and which set of trace engine registers to use. The trace engine device control registers are used to determine where to write the data into the trace buffer. The APU stalls a CPU instruction stream pipeline while the data is written and the trace buffer pointers are being updated, making the instruction atomic.

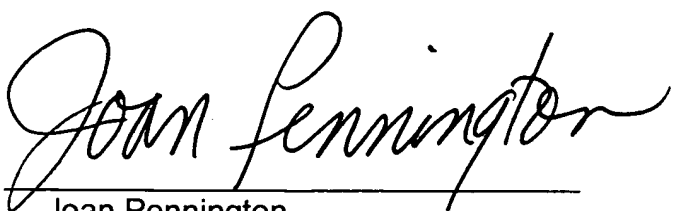
Dependent claims 3-10, 12-14, and 16-18 respectively depend from patentable claims 1, 11, and 15, further defining the invention. Each of the dependent claims 3-10, 12-14, and 16-18, as amended, is likewise patentable.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-18, as amened, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

By: 

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